CLAIMS

What is claimed is:

1. A method comprising:

receiving one or more write commands and their corresponding write data from a first device, the corresponding write data being delayed by the first device by a first delay period;

storing the one or more write commands and their corresponding write data in a set of buffers; and

upon receiving another write command from the first device, sending a buffered write command and its corresponding write data to a second device for execution, without waiting for the write data corresponding to said another write command to be sent from the first device.

2. The method of claim 1 wherein the first delay period corresponds to a read latency of a previous read command.

3. The method of claim 1 wherein the buffers comprises a first buffer to store the respective write data, a second buffer to store row addresses corresponding to the respective write commands, and a third buffer to store column addresses corresponding to the respective write commands.

4. The method of claim 1 wherein the buffered write commands are executed by the second device on a first-in-first-out basis.

5. The method of claim 4 wherein, upon receiving said another write command from the first device, an oldest write command stored in the buffers is popped from the buffers and sent to the second device for execution and said another write command is pushed onto the top of the buffers.

6. The method of claim 1 wherein the first device comprises a memory controller and the second device comprises one or more memory devices.

7. The method of claim 6 wherein the first device comprises a RAMBUS memory controller that operates according to RAMBUS memory control specification

8. The method of claim 6 wherein the second device comprises one or more synchronous dynamic random access memory (SDRAM) devices that operate according to SDRAM specification.

9. The method of claim 1 further comprising:

receiving a new read command from the first device;

determining whether a read address associated with the new read command matches a write address associated with a write command stored in the buffers; and

if there is a match, performing a read bypass operation to use the corresponding write data stored in the buffers as read data for the new read command instead of data stored in the second device.

10. The method of claim 9 wherein the read address and the write address each comprises a respective row address and a respective column address.

11. The method of claim 10 wherein determining comprises:

comparing the row address associated with the new read command to the row address associated with the write command; and

comparing the column address associated with the new read command to the column address associated with the write command.

12. The method of claim 9 wherein performing the read bypass operation comprises:

selecting the corresponding write data from the buffers; and

transmitting the corresponding write data to the first device as read data for the new read command.

13. An apparatus comprising:

a set of buffers to store one or more write commands and their corresponding write data received from a first device, the corresponding write data being delayed by the first device by a first delay period, wherein, upon receiving another write command from the first device, a buffered write command and its corresponding data are sent to a second device for execution, without waiting for the write data of said another write command to be sent from the first device.

14. The apparatus of claim 13 further comprising:

logic to perform a read bypass operation, comprising:

logic to determine whether a read address associated with a new read command received from the first device matches a write address associated with a write command stored in the buffers; and

logic to use the corresponding write data stored in the buffers as read data for the new read command instead of data stored in the second device if there is a match.

15. The apparatus of claim 14 wherein the read address and the write address each comprises a respective row address and a respective column address.

16. The apparatus of claim 15 wherein logic to determine comprises:

a first comparator to compare the row address associated with the new read command to the row address associated with the write command; and

a second comparator to compare the column address associated with the new read command to the column address associated with the write command.

17. The apparatus of claim 14 wherein logic to perform read bypass operation further comprising:

a multiplexor to select the corresponding write data from the buffers; and

logic to transmit the corresponding write data to the first device as read data for the new read command.

18. The apparatus of claim 13 wherein the buffers comprises a first buffer to store the respective write data, a second buffer to store row addresses corresponding to the respective write commands, and a third buffer to store column addresses corresponding to the respective write commands.

19. The apparatus of claim 13 wherein, upon receiving said another write command from the first device, an oldest write command stored in the buffers is popped from the buffers and sent to the second device for execution and said another write command is pushed onto the top of the buffers.

20. The apparatus of claim 13 wherein the first device comprises a memory controller and the second device comprises one or more memory devices.

21. The apparatus of claim 13 wherein the first delay period corresponds to a read latency of a previous read command.

22. A memory control unit comprising:

a first memory controller that issues read and write commands to access a first memory device, the first memory controller deferring write data transfer on a write command for a period corresponding to a read latency of a previously issued read command, the first memory device requiring write data to be sent with a write command to execute a write operation to store the respective write data into the first memory device; and

a translator unit coupled to the first memory controller and the first memory device to provide signal translation between the first memory controller and the first memory device to facilitate memory transactions between the first memory controller and the first memory device, the translator unit including a set of buffers to store one or more write commands and their corresponding write data received from the first memory controller, the translator unit to send a buffered write command and its corresponding write data to the first memory device for execution upon receiving another write command from the first memory controller, without waiting for the write data corresponding to said another write command to be sent from the first memory controller.

23. The memory control unit of claim 22 wherein the translator unit further includes logic to perform read bypass operation comprising:

logic to determine whether a read address associated with a new read command received from the first device matches a write address associated with a write command stored in the buffers; and

logic to use the corresponding write data stored in the buffers as read data for the new read command instead of data stored in the second device if there is a match.

24. The memory control unit of claim 23 wherein the read address and the write address each comprises a respective row address and a respective column address.

25. The memory control unit of claim 24 wherein logic to determine comprises:

a first comparator to compare the row address associated with the new read command to the row address associated with the write command; and

a second comparator to compare the column address associated with the new read command to the column address associated with the write command.

26. The memory control unit of claim 24 including:

a multiplexor to select the corresponding write data from the buffers as read data for the new read command.

27. The memory control unit of claim 22 wherein the set of buffers comprises:

a first buffer to store write data associated with write commands received from the first memory controller;

a second buffer to store row addresses associated with write commands received from the first memory controller; and

a third buffer to store column addresses associated with write commands received from the first memory controller.

28. A system comprising:

one or more processors;

a system memory; and

a memory control unit coupled to the one or more processors and the system memory, the memory control unit comprising:

a memory controller; and

a translator unit coupled to the memory controller to provide an interface between the memory controller and the system memory, the translator unit comprising:

a set of buffers to store write commands and corresponding write data received from the memory controller in which a buffered write command and its corresponding write data are sent to the system memory for execution upon receiving another write command from the memory controller.

29. The system of claim 28 wherein the translator unit further comprises:

read bypass logic comprising:

logic to determine whether a read address associated with a subsequent read command received from the first device matches a write address associated with a write command stored in the buffers; and

logic to use the corresponding write data stored in the buffers as read data for the subsequent read command instead of data stored in the second device if there is a match.

30. The system of claim 28 wherein the memory controller defers sending write data associated with a write command for a period corresponding to a read latency of a previously issued read command and wherein the system memory requires that write data associated with a write command be sent with the respective write command to the system memory for the system memory to perform a corresponding write operation.